Amendments to the Drawings

A proposed correction to Figure 1 has been made as required by the Examiner to avoid abandonment of the application.

Attachment: Annotated Marked-Up Drawings

REMARKS

The remainder of this reply is set under appropriate sub-headings for the convenience of the Examiner.

Claims Amendments

Claim 1 has been amended to include the additional limitation that the heterostructured field effect transistor has a plurality of gates, wherein the gates have a trapezoidal cross-section. Support for this amendment can be found in the specification at page 5, lines 12-15 and in Fig. 1. Dependent Claim 8 has been canceled.

Other amendments have been made to the claims in order to correct minor informalities, and support for these amendments is self-evident.

No new matter has been added.

Objections to the Drawings

Examiner objected to the drawing because the claimed subject matter recites that "the gate voltages being individually biased to tailor the potential field" and "the tailoring occurs" to create uniform distribution of energy subbbands, and that the drawing failed to clearly show how the individual gates were biased, or applied, as now claimed. The Examiner stated that these features must be canceled from the claims or shown in the drawing.

37 C.F.R. § 1.83(a), which was recited by the Examiner, states "the drawing in a nonprovisional application must show every feature of the invention specified in the claims." However, nothing under 35 U.S.C. § 113, nor under the Rules of Practice (37 C.F.R.), requires that subject matter that does not admit of illustration be included in a drawing. For example, as stated by 35 U.S.C. § 113:

> The applicant shall furnish a drawing where necessary for the understanding of the subject matter sought to be patented. When the nature of such subject matter admits of illustration by a drawing and the applicant has not furnished such a drawing, the

> Director may require its submission within a time period of not less than two months from the sending of a notice thereof.

Similarly, 37 C.F.R. § 1.81(c) states:

> Whenever the nature of the subject matter sought to be patented admits of illustration by a drawing without its being necessary for the understanding of the subject matter and the applicant has not furnished such a drawing, the examiner will require its submission within a time period of not less than two months from the date of the sending of a notice thereof.

The (now) claimed features identified by the Examiner, namely that "the gate voltages being individually applied to tailor the potential field" and "the tailoring occurs," do not admit of illustration in a drawing. Rather, they are inherent to the claimed subject matter. Further, illustration of these features in a drawing is not necessary for an understanding of the subject matter to be patented. Therefore, the drawings meet the requirement of 35 U.S.C. § 113 and 37 C.F.R. § 1.83(a).

In order, however, to avoid abandonment of the application, Applicants herewith attach proposed drawing corrections to comply with the requirement of the Office Action.

Claim Objections

Claims 1-13 were objected to for various informalities and/or defects, including lack of antecedent basis. In addition, Claim 1 was objected to for reciting the term of "the potential field," but without clearly specifying where the field is observed.

Claim 1 has been amended to state that the gate voltages are individually applied to tailor a potential along a channel of the transistor. Support for this amendment can be found at page 5, lines 1-8.

Claims 4, 6 and 7 are objected to by the Examiner as reciting the term "along the channel."

Figure 1 is clearly represented as a cross-section of a heterostructural field effect transistor of the invention. Page 5, lines 19-21 specify that, with respect to Figure 1, gates 12 are

optically patterned and realized with a Ti/Pt/Au metal lift-off process in a double recessed channel. One skilled in the art would understand from the figure and the recited portion of the specification that the figure also represents a cross-section of the channel. The phrase "along the channel" clearly means in a direction parallel to a major axis of the channel and, therefore, the direction indicated by the phrase with respect to Figure 1 is a direction that is normal to the cross-section represented in Figure 1. The meaning of the language of Claims 4, 6 and 7 with respect to the phrase "along the channel" in view of the specification and with reference to Figure 1 is clear.

Examiner also objected to lack of antecedent basis for the limitations "the heterostructure barrier" in Claim 6 and "the 2D electron gas barrier" in Claim 7. Claims 6 and 7 have both been amended to correct these defects.

Reconsideration and withdrawal of the objections raised by the Examiner respectfully is requested.

Rejections of Claims Under 35 U.S.C. § 112, First Paragraph

Claims 1-13 are rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. In particular, the Examiner stated that certain phrases in the claims lack adequate description because, according to the Examiner, there is insufficient description of how individual gate voltages are individually biased and how individually biased potential relationships can be maintained under various conditions. With respect to Claim 5, the Examiner stated that " it is not clear how an electron can be accelerated by the uniform potential" because "the electric field strength would be zero in such a uniform potential."

The specification clearly states how the voltage of the gates and the tri-gate structure is applied in a manner that makes the heterostructure potential uniform. For example, at page 5, line 29 through page 6, line 4:

> The variation of electron energies are minimized by making the width of the heterostructure barrier more uniform along the channel. This is accomplished by tailoring the field, that is, by making the slope of the 2D electron gas barrier more uniform along the channel. This allows the electrons to be energetic at the

> source, while not exceeding the energies that cause hot electron damage.

With respect to Claims 5, the limitations that "the uniform potential accelerates electrons as they are injected into the channel." As cited above, tailoring the field "allows the electrons to be energetic at the source, while not exceeding the energies that cause electron damage." Therefore, although electrons may not accelerate in a uniform potential field, they accelerate, as stated in Claim 5, "as they are injected into the channel."

One skilled in the art would understand that the specification provides a written description of the subject matter of Claims 1-13 that is in compliance with the first paragraph of 35 U.S.C. § 112. Therefore, reconsideration and withdrawal of this rejection respectfully is requested.

Rejection of Claims Under 35 U.S.C. § 102(b)

Claims 1-10 and 13 are rejected under 35 U.S.C. § 102(b) as being anticipated by Boos, *et al.* (Boos *et al.*; Reduction of Gate Current in AlSb/InAs HEMTs Using a Dual Gate Design, Electronics Letters, Vol. 32, No. 17, August 15, 1996). The Examiner stated that Boos, *et al.* disclose a heterostructured field effect transistor within the scope of Claim 1 and that, with respect to at least some of the conditions, the individual gates can "naturally produce substantially improved uniformities in potential, in distribution of energy subbands, in width of the heterostructure barrier, and/or in the slope of the 2D electron gas barrier, compared with the case of a single-gate configuration."

With respect to Claim 13, the Examiner stated that "the transconductance of the transistor" of Boos, *et al.* can be naturally substantially linear over a range of the gate voltages, compared with the case of a single-gate configuration."

Claim 1 has been amended to specify that the gates of the heterostructured field effect transistor have a trapezoidal cross-section. Support for this amendment can be found in the specification at page 5, lines 12-15:

> In the illustrated embodiment, transistors with the special trapezoidal gate design are used, such as the gates 12 shown in

Figure 1. The trapezoidal shape of the gates and the top metalization allows placing two sub-micron gates very close together, with improves the efficiency of tailoring.

There is no disclosure of suggestion in Boos, *et al.* of employing gates that are trapezoidal in cross-section. Therefore, Claim 1, and dependant Claims 2-7, 8-10 and 13, which depend directly or indirectly from independent Claim 1, also are not anticipated by Boos, *et al.* Therefore, reconsideration and withdrawal of the rejection respectfully is requested.

Rejection of Claims Under 35 U.S.C. § 103(a)

Claims 11 and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Boos, *et al.*, in view of Jean, *et al.* (Jean, *et al.*; FR25550889). In particular, the Examiner stated that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the transistor of Boos, *et al.* with three of four gates being formed therein, per the teachings of Jean, *et al.*, so that a transistor with improved channel performance would be obtained."

Jean, *et al.* do not remedy the deficiencies of Boos, *et al.* Specifically, there is no disclosure or suggestion in Jean, *et al.* of employing gates having a trapezoidal cross-section. Therefore, neither Boos, *et al.* nor Jean, *et al.*, taken either separately or in combination, disclose or suggest the subject invention of Claims 11 and 12. Therefore, the requirements of 35 U.S.C. § 103(a) are met by the invention of Claims 11 and 12 in view of these references.

Reconsideration and withdrawal of this rejection also respectfully is requested.

CONCLUSION

As required, Applicants submit herewith proposed drawing corrections to overcome the objection under 37 C.F.R. § 1.83(a). Also, the claims have been amended as necessary to overcome objections raised by the Examiner. Further, as amended, the claims meet the requirements under 35 U.S.C. § 112, first paragraph, section 102(b) in view of Boos, *et al.*, and section 103(a) in view of Boos, *et al.*, and Jean, *et al.*, taken either separately or in combination.

Reconsideration and withdrawal of all objections and rejections is respectfully requested. If the Examiner would like to discuss these matters in greater detail, he is respectfully requested to contact the undersigned attorney.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By Robert T. Conway 33,859 for
N. Scott Pierce
Registration No. 34,900
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
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ATTACHMENT
PROPOSED DRAWING CORRECTION

CROSS SECTION OF FET WITH THREE TRAPEZOIDAL GATES
FIG 1

The gate voltages are individually applied to tailor the potential field 10

The tailoring occurs along a channel of the light electron mobility transistor to create a uniform distribution of energy subbands.